

## Effectiveness of PCB Simulation in High Speed DDR Memory Design

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### **Abstract**

Signal integrity for high speed DDR memory design at the printed circuit board (PCB) level is very essential and important for making a robust design .This paper describes how simulation tools can be helpful for choosing best termination method and other signal integration parameter along with the design process .A Simulation tool Hyperlynx has been used for high speed digital design for DDR2 in this paper. We present DDR 2 design example in which the main approach is to get wide opened eye with minimum level of overshoot and undershoot. Hyperlynx like tools can be used at different level of design to make a robust and reliable design work.

### **I. INTRODUCTION**

Signal Integrity is essential when we talk about designing high speed digital circuits like memories [1-3].At high clock rates and dual edge data transfer maintaining signal integrity and system reliability is a tough job to do. Topic Related to DDR design signal integrity often include noise and timing margins, models for drivers and receivers , transmission lines ,load terminations ,crosstalk due to capacitive and inductive coupling and ground and power noises. High speed DDR interface circuit simulation in Hyperlynx use very accurate [4]I/O buffer Interface Specifications .The use of I/O buffer Interface Specifications(IBIS) has gained widespread acceptance .[5]There are three main areas of concern when developing high-speed design constraints: signal quality, timing, and crosstalk. Signal quality includes

Items like overshoot, ring back, and non monotonic ties: items that can damage a receiver or introduce data errors. Timing at the PCB level, including effects of terminations, receiver loading, and trace impedances and lengths, must be rigorously analyzed to ensure compliance at the system level.[6] Crosstalk, which is unwanted noise induced by one trace onto another, can affect both signal quality and timing. Ensuring proper system operation requires all of these analyses. The resulting constraints drive trace lengths, topology, and spacing. This, in turn, drives items such as parts placement. It is also necessary to constrain items such as board stackup, trace widths and copper weights. Clearly, a highspeed PCB design cannot even begin without the proper analysis. HyperLynx from Mentor Graphics makes this analysis quick and easy. The tool contains different levels for simulating design. Pre and post verification of the

result can also be done in this tool which insures the robust and reliable design for a design engineer and these results are very close to the bench level tests .

## II. SIGNAL QUALITY OF DDR SIGNALS

Data is reduced to a series of 1s and 0s which we represent by high and low in real time systems .[5]There are logic threshold of the receiver which determines that whether the voltage it is receiving is 0 or 1.So a voltage above the threshold is considered as 1 and voltage below the threshold level is considered as 0 .Also the low and high voltage must be in limits of the receiver maximum acceptable voltages otherwise it can damage the system So a designer has to take care of the two fundamental constraints in signal quality analysis which are ringback.If a designer has to just connect a data bus of the DDR ,the result would be something like the waveform shown in figure 1.[7]Here we can see there are both ringback and overshoot violations. The blue waveform which is the receiver in the right of the topology shows positive overshoot in excess of 0.5V. Also we can see the signal is ringback to 0.7v which is the lower logic threshold so this can lead to errors in the data stream of the processor and DDR and also the receiver can be damaged too. If length of the trace is reduced significantly ,to well below the signal edges these receiver waveforms get cleaned a bit as shown in figure 2.However such lengths are typically on the order of less than inch in DDR circuits and not feasible in the design .

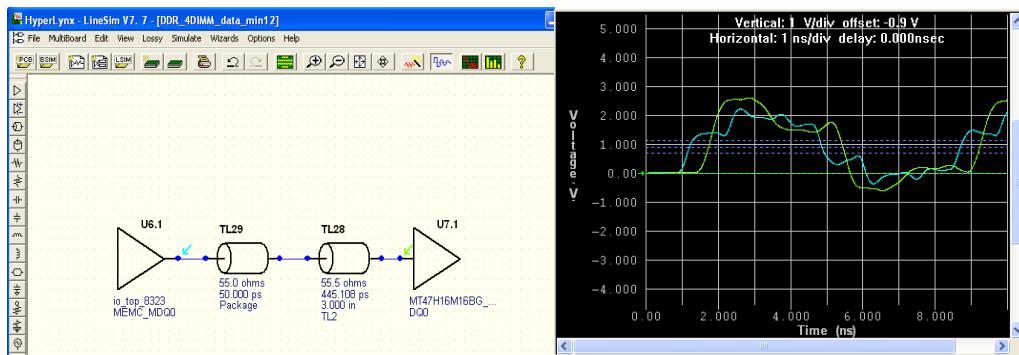


Figure 1: A DDR topology with signal quality problems

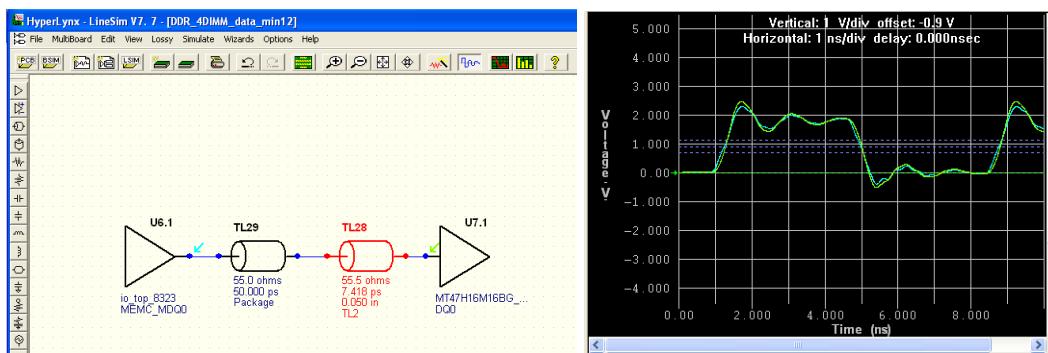
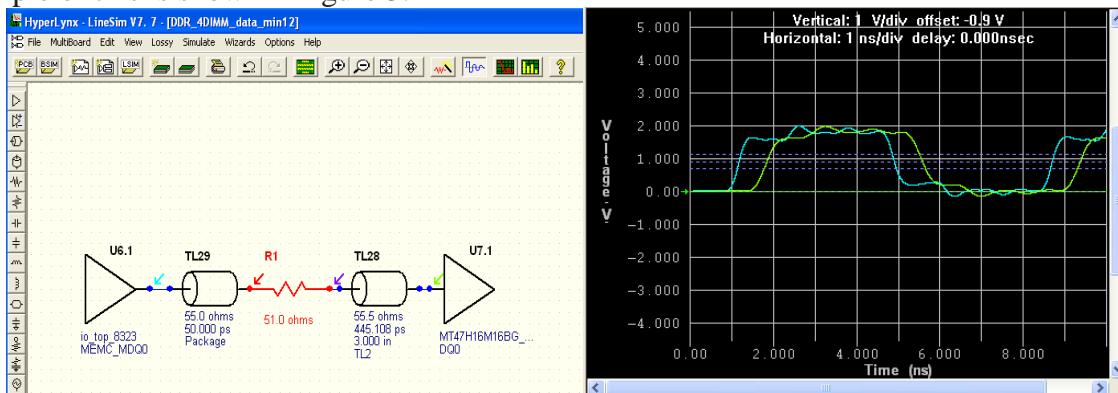


Figure 2: A reduced length topology with clean signals

Another method of improving the signal quality at the receiver is to use terminations, Which matches the impedance of the driver and receiver to the board traces, controlling the reflections and overshoot violations . We can have the more length of the traces as terminations give us the flexibility to do it.The Hypelynx can guide for choosing a termination scheme and the value for the termination too so a designer can put the nearest value available in the market .Also the location of the termination can vary and fixed for the best cleaned signal by analyzing results. An example of this is shown in figure 3.



**Figure 3:** A terminated DDR Data Bus with clean signals.

### III. TIMING CONSTRAINT

In the receivers data is clocked in at certain levels [8].When the data is not there when the system need to be, it the system does not work There are two type of common clock buses used – common clock and source synchronous, which lead to two type of layout constraints, min/max and matched lengths. As in DDR for proper working of the data the data bus delay should have some correlation with data clock. Which did not violate the hold time requirement of the receiver .This is called minimum and maximum length constraints .So the other hard constraint to implement in the DDR design is the matched delay of data and data strobe signals

### IV. CROSSTALK

Spacing between Traces is the important constraint for the layout of DDR design [9] .This is determined by the amount of crosstalk that occur between signals. Crosstalk can be influence by edge rate of the driver, board stackup, amount of parallelism between traces and spacing between traces .

Hyperlinux Field solver can estimate the crosstalk between signals and areas where it is maximum and minimum. Crosstalk affects badly on both timing and signal quality of the DDR signals. An example of crosstalk simulation is shown in figure 4 .With all the information needed like stackup information ,models if transmitter and receiver ,we can adjust the spacing between traces to determine an acceptable level of crosstalk .So in DDR we generally follow 3W spacing rule where "W" Is the with of the track.

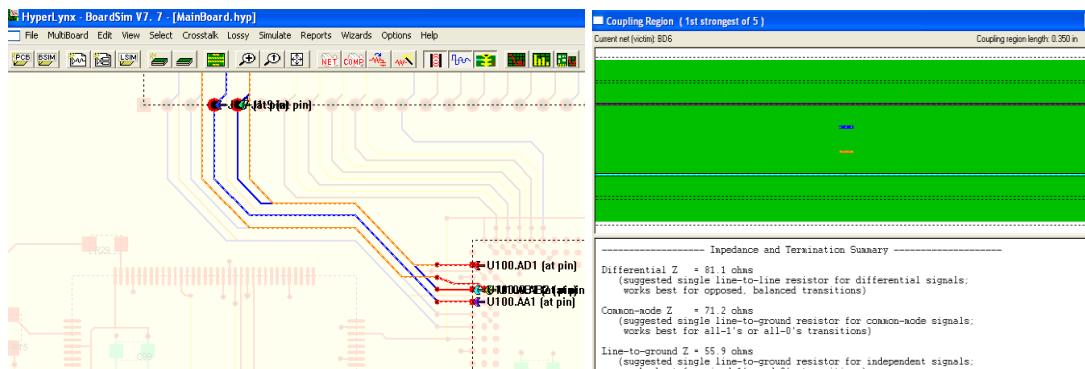


Figure 4: Crosstalk analysis in HyperLynx

## V. POST-ROUTE VERIFICATION

After all constraints has been followed and routing has been done [5], it is useful to verify that board meets the original electrical requirement which prompted these constraints. To verify all the traces and close the loop the Hyperlynx include the post routing simulation which can be done in batch mode. In figure 6 note that Boardsim runs a simulation directly on the layout data and verify against overshoot, delay, and crosstalk constraints. If one of the net find violating the constraint that net can be checked one at a time.

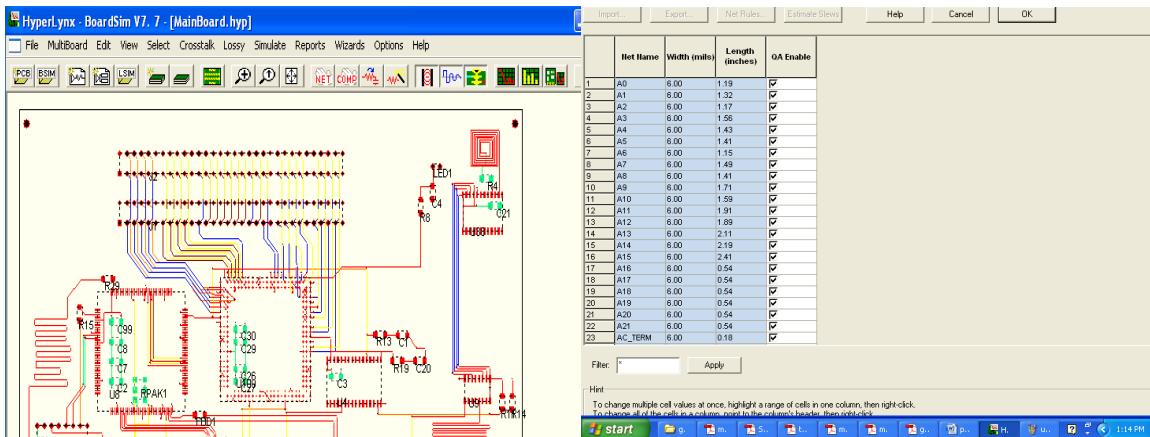


Figure 5: A simple DDR board in BoardSim with the associated electrical constraints

## VI. CONCLUSION

An example of DDR design by LineSim of Hyperlynx and BoardSim of Hyperlynx are presented in which results of simulation has been shown. Our experience has shown that LineSim and Boardsim is an effective tool which helps designers for maintaining signal integrity and timing constraints.

Hyperlynx is a valuable and necessary tool for making high speed designs like DDR and PCI buses .It can help the designer on different levels of design and also have the ability to do post routing checks. The results are very close to the actual bench level tests and make the design process fast and the time to market of the product has been improved by using these types of tools.

## VII. REFERENCES

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